REMARKS

Applicants respectfully traverse and request reconsideration. Applicants would again like to thank the Examiner for allowing claim 40 and for indicating that claims 7 through 12, 14, 16 and 17 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 21 through 23 and 25 through 27 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,040,845 (Melo).

In making the rejection to independent claim 21, the Office Action fails to cite to or otherwise specifically show where Melo teaches, among other things 1) an internal I/O circuit, 2) a bus bridge signal and 3) an internal bus bridge. If the rejection is maintained, Applicants request a showing by column and line number pursuant to 37 C.F.R. § 1.104 as to where the reference allegedly teaches these cited elements as the current Office Action fails to indicate where these elements are taught.

Melo is directed to a computer system including a processor 12 coupled to a north bridge 14 and south bridge 28. Both the north bridge 14 and south bridge 28 are external to the processor 12. According to the Office Action, the claimed "internal circuit" is equated to processor 12 of FIG. 1. However, the Office Action also equates the "internal circuit" with north bridge 14 and south bridge 28. In the event the Office Action intended to equate the claimed "internal bus bridge" rather than the "internal circuit" with the north bridge 14 and south bridge 28 of FIG. 1, such an assumption is made herein. Accordingly, an appropriate clarification is requested. The claimed "any external circuit" is equated to external I/O devices 32A and 302B. In rejecting claim 21, the Office Action merely makes reference to "Melo's internal I/O circuit" rather than cite to a column and line number or even to a figure in Melo for teaching an internal I/O circuit.

In contrast, the claims recite, among other things, "at an internal I/O circuit, preventing signals from any external circuit from reaching the internal circuit." According to the response to arguments on page 13 of the Office Action, the Examiner appears to misunderstand the claim limitation "internal." The specification repeatedly describes the claim limitation as on-chip. (Specification page 4, line 24, page 12, line 11 and page 18, lines 7- through 11). Therefore, the claimed "at an internal circuit", "the internal bus bridge" and "the internal I/O circuit" are all on-chip. However, FIG. 1 in Melo explicitly shows north bridge 14 and south bridge 28 external to the processor 12. As a result, the "internal bus bridge" (equated to north bridge 14 and south

bridge 28) are external to the internal circuit (equated to processor 12) rather than internal to the processor 12. Since the Office Action equates the claimed "internal circuit" with the processor 12, the Office Action improperly equates the claimed "internal bus bridge" with north bridge 14 and south bridge 28 because north bridge 14 and south bridge 28 are explicitly shown external to processor 12 in FIG. 1. Therefore, among other things, the Office Action fails to show where Melo teaches "an internal bus bridge." Further, the Office Action fails to show where Melo teaches "at an internal circuit, receiving a bus bridge signal from an internal bus bridge." Since the claimed "internal circuit" is equated to processor 12 and the claimed "internal bus bridge" is equated to north bridge 14 and south bridge 28 and since north bridge 14 and south bridge 28 are shown explicitly as external to processor 12, the internal circuit necessarily fails to "receive a bus bridge signal from an internal bus bridge." For at least these reasons, Melo fails to teach all the elements as arranged in claim 21, including, among other things, "at an internal circuit, receiving a bus bridge signal from an internal bus bridge; and at an internal I/O circuit, preventing signals from any external circuit from reaching the internal circuit." Therefore, Melo fails to teach all the elements as arranged in claim 21 and as a result, the Office Action fails to show how Melo anticipates claim 21. Reconsideration and withdrawal of the present rejection is requested.

Claims 21 through 23, 25 through 27, 29 through 33 and 35 through 38 are rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,141,021 Bickford.

Bickford is directed to a video system 100 including an accelerator graphics port (AGP) bus 110 coupled to an AGP graphics accelerator chip 118 and an AGP graphics accelerator add-in card 122. (Bickford ¶ 4, lines 33–49.) A disable device 124 selectively disables transmitting on either the video down AGP graphics accelerator 118 or the add-in AGP card 122 for avoiding simultaneous transmissions on the accelerator graphics port (AGP) bus 110. (Bickford ¶ 4, lines 46–49.) Thus, two AGP accelerators 118, 122 may be *simultaneously coupled to the AGP 110* and therefore both always receive signals on the AGP 110. The disable device 124 merely disables one of the AGP graphics accelerators 118, 122 and prevents both devices 118, 122 from contending for transmission on the AGP bus 110. (Bickford col. 4, lines 49–53.)

In contrast, claim 21 recites "at an internal I/O circuit, preventing signals from any external circuit from reaching the internal circuit." However, Bickford explicitly teaches an opposite approach, namely preventing simultaneous transmissions on the AGP bus 110 by merely disabling either AGP graphics accelerator 118 or the AGP add in card 122. Rather than teach both "preventing signals from any external circuit from reaching the internal circuit,"

Bickford teaches that the AGP graphics accelerator 118 and the AGP add in card 122 (via the AGP add in card connector 120) simultaneously receive all data signals on AGP bus 110 as explicitly described in Bickford col. 4, lines 49-53 and as explicitly shown in FIG. 3. For example, FIG. 3 shows all devices including AGP add in card 122 via the AGP add in card connector 120 as well as the AGP graphics accelerator 118 are coupled to AGP bus 110 and therefore receive all signals on AGP bus 110. The disable device 124 merely disables either the device 118 or device 122 from transmitting on AGP bus 110. As a result, Bickford fails to teach, among other things, "preventing signals from any external circuit from reaching the internal circuit."

Further, the Office Action fails to show where Bickford teaches that the claimed internal circuit, internal bus bridge and the internal I/O circuit are all "internal" as previously described. For at least these reasons, the Office Action fails to show where Bickford teaches "at an internal circuit, receiving a bus bridge signal from an internal bus bridge; and at an internal I/O circuit, preventing signals from any external circuit from reaching the internal circuit." Consequently, Bickford fails to teach all the elements as arranged in claim 21 and as a result Bickford fails to anticipate claim 21. Reconsideration of the present rejection is respectfully requested.

As to claims 22, 23, 26, 27, 30 through 33, 35, 37 and 38, Applicants respectfully reassert the relevant remarks made above with respect to claim 21. Further, these claims contain further patentable subject matter and are allowable not merely as being dependent upon an allowable base claim. As such, reconsideration and withdrawal of the present rejection is respectfully requested.

Further, claim 21 recites "at an internal I/O circuit, preventing signals from any external circuit from reaching the internal circuit." As a result, claim 21 requires that an internal I/O circuit prevents signals from any external circuit from reaching the internal circuit. Nevertheless, the Office Action equates the disable device 124 of Bickford to the internal I/O circuit. Rather than describe an internal I/O circuit, Bickford states that the disable device 124 is a jumper or selector switch. (Bickford col. 5, lines 25 through 30). Bickford explicitly teaches that the disable device such as a jumper is a metal bridge that closes an electrical circuit. As a result, the disable device 124 of Bickford as cited in the Office Action fails to describe, among other things, "an internal I/O circuit."

As to claim 29, Applicants respectfully reassert the relevant remarks made above with respect to claim 21 and note that Bickford does not teach, among other things, an integrated bus

bridge graphics unit, coupled to the memory bus, further including an internal circuit operably configured to avoid signals from an external graphics bus. Instead, Bickford, as previously stated, teaches enabling and disabling the AGP graphics accelerators 116, 118, 120, 122. For example, Bickford simply controls the receipt of a frame # signal from the PCI bus to either of the two graphics controllers to enable or disable one of the two graphics controllers. Since Bickford teaches that the internal graphics bus is coupled directly to the external slot and to the internal AGP graphics chip (see Figure 3), the internal circuit always receives signals from the external graphics path or bus, rather than "an internal circuit operably configured to avoid signals from the external graphics buses." Consequently, Bickford fails to anticipate claim 29. As such, reconsideration and withdrawal of the present rejection is respectfully requested.

Claim Rejections under 35 U.S.C. § 103

Claim 1 is rejected under 35 U.S.C. § 103(a) based on U.S. Patent No. 5,621,900 (Lane) in view of U.S. Patent No. 5,633,599 (Kubota) or U.S. Patent No. 5,850,530 (Chen).

With regards to claim 1, Applicants submit that since amended claim 1 includes the limitations of dependent claims 2 and 7 and since the Office Action has indicated that claim 7 is allowable if written in independent form, claim 1 is therefore allowable.

Claims 1 through 5, 13, 15, 18 through 20, 24, 34 and 41 through 43 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Bickford in view of Kubota or Chen. Applicants repeat the relevant remarks above. Claim 1 is also rejected under 35 U.S.C. § 103(a) based on Melo in view of Kubota or Chen. As previously stated, according to the Office Action, claim 7 is allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claim. Therefore, claim 1 is amended to include the limitations of claims 2 and 7. As a result, amended claim 1 is allowable.

With regards to claims 3 through 5, 13, 15 and 18 through 20, these claims are all allowable for at least the reason that independent claim 1 is allowable. Applicants also submit that the dependent claims are allowable in light of the presence of novel and nonobvious elements contained in these claims that are not otherwise present in the independent claims.

With regards to claim 41, the Office Action acknowledges that Bickford does not disclose an input buffer. Further, since Bickford teaches disable device 124 to disable either the AGP accelerator 118 or the add-in card 122 and thus perform bus selection, modifying Bickford to add an input buffer would be redundant and therefore unnecessary. Therefore, one would not be

motivated to modify Bickford to add the input buffer as asserted. Consequently, the Office Action fails to establish a prima facie case of obviousness. As a result, the rejection of claim 41 is improper.

The Office Action also fails to show where the combination of Bickford, Kubota and Chen teach, among other things, "to isolate the first internal signal on the first internal signal path from the first external signal." Therefore, Office Action fails to show where the references as combined teach each and every element as arranged in the claims. If the rejection is maintained, Applicants request a showing by column and line number as to which reference allegedly teaches the cited elements as the current Office Action fails to indicate where these elements are taught pursuant to 37 C.F.R. § 1.104.

With regards to claims 42 and 43, Applicants submit that the dependent claims are allowable in light of the presence of novel and nonobvious elements contained in these claims that are not otherwise present in independent claim 41. Therefore, claims 42 and 43 are allowable for at least the reasons the independent claims are allowable.

As to claims 3, 4, 5, 13, 15, 18 through 20, 24 and 34, Applicants respectfully reassert the relevant remarks made above and again note that these claims add new and nonobvious subject matter. Further, these claims are allowable for at least the reasons that claims 1, 21, and 29 are allowable. As a result, these claims are believed to be in condition for allowance.

Claims 6, 28 and 39 are rejected under 35 U.S.C. § 103(a) based on Bickford in view of the NGP protocol or U.S. Patent No. 4,529,840 (Colton).

With regards to claim 6, claim 6 is dependent on claim 3 which depends on amended claim 1. Therefore, claim 6 is allowable at least for the reasons claims 1 and 3 are allowable. Further, the unsupported assertion in the Office Action that it would have been obvious to one having ordinary skill in the computer art adapt the NGP protocol into Bickford fails to establish sufficient motivation for one skilled in the art to modify Bickford. For at least this reason the Office Action fails to establish a prima facie case of obviousness for claim 6.

With regards to claim 28 and 39, Applicants repeat the above remarks, especially with respect to claim 6 showing that the Office Action fails to establish sufficient motivation for one skilled in the art to modify Bickford. As a result, the Office Action fails to establish a prima facie case of obviousness for claim 28 and 39. Further, claims 6, 28 and 39 include new and nonobvious subject matter and are believed to be in condition for allowance. Reconsideration and withdrawal of the current rejection is respectfully requested.

CONCLUSION

Applicant respectfully submits that the Claims are in condition for allowance and requests that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

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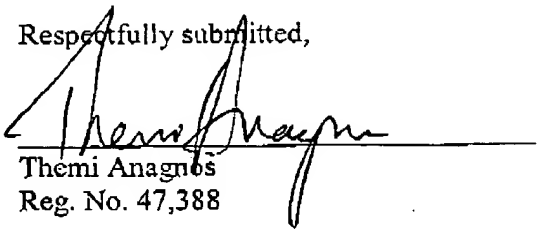
Respectfully submitted,



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